Development of Analytical Compact Drain Current Model For 28nm FDSOI MOSFETs

T. A. Karatsori, A. Tsormpatzoglou, C. G. Theodorou, E. G. Ioannidis, S. Haendler, N. Planes, G. Ghibaudo, *Fellow, IEEE* and C. A. Dimitriadis, *Member, IEEE*

***Abstract*— An analytical drain current compact model for lightly doped short-channel ultra-thin body and box fully depleted silicon-on-insulator MOSFETs with back gate control, which includes the effects of drain-induced barrier lowering, channel-length modulation, saturation velocity, mobility degradation, quantum confinement, velocity overshoot and self-heating, is presented. A comparison is performed with experimental transfer and output characteristics of devices with channel lengths 30 and 240 nm and with back bias varying from -3 to +3 V. The good accuracy of the model makes it suitable for implementation in circuit simulation tools.**

***Index Terms*—Back-gate control, compact model, FD-SOI UTBB MOSFETs.**

I. Introduction

Ultra-thin body and box (UTBB) fully depleted silicon-on-insulator (FD-SOI) MOSFETs are considered as one of the best candidates for control of short channel effects (SCEs) in future sub-28 nm CMOS generations [1], because they provide process simplicity compared to FinFETs, a threshold voltage control with back gate bias and lower variability phenomena due to random dopant fluctuations [2].

To exploit the benefits of UTBB FD-SOI MOSFETs with back bias control, an analytical, accurate and fast compact model that describes properly the transistor behavior for a wide range of back bias is required. In previously reported works on compact models of asymmetric independent double-gate MOSFETs, the models are based on numerical techniques [3]-[6], resulting in a poor speed of simulation. Recently, a computationally efficient model has been presented, providing accurate results when the back gate is biased in the reverse and low forward bias range [7]. For the case where a strong forward back bias is applied, a surface potential compact model has been proposed, utilizing complicated equations while fundamental effects (such as velocity overshoot and self-heating) were not considered [8].

Recently, we developed simple analytical models for the threshold voltage and ideality factor of the front interface for asymmetrical UTBB FD-SOI MOSFETs [9]. In this paper, we have improved our previous model and derive a complete analytical charge-based compact drain current model valid in all regions of operation with back gate control, including the drain-induced barrier lowering (DIBL), channel-length modulation (CLM), saturation velocity, mobility degradation, quantum confinement, velocity overshoot (VO) and self-heating (SH) effects.

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T. A. Karatsori, A. Tsormpatzoglou, and C. A. Dimitriadis are with the Department of Physics, Aristotle University of Thessaloniki, 54124 Thessaloniki Greece (email: cdimitri@physics.auth.gr).

T. A. Karatsori, C. G. Theodorou, E. G. Ioannidis, and G. Ghibaudo are with the IMEP-LAHC Lab. in Minatec, Parvis Louis Néel, 38016 Grenoble Cedex 16, France.

S. Haendler and N. Planes are with STMicroelectronics, 38921 Crolles, France.

II. Devices under study

The devices measured in this work are n-MOS transistors with back-plane, issued from 28 nm FD-SOI CMOS technology, fabricated by STM, France [10]. The device characteristics are shown in Table I.

TABLE I
DEVICE PARAMETERS OF THE MEASURED DEVICES

Parameter	Definition	Value	Units
N_A	doping concentration of the channel	10^{15}	cm^{-3}
N_{SD}	doping concentration of the source/drain contacts	10^{20}	cm^{-3}
t_{ox}	Equivalent front oxide thickness	1.55	nm
t_{BOX}	Burried oxide thickness	25	nm
t_{Si}	silicon film thickness	7	nm

III. Model development

As indicated in [11], the threshold voltage of advanced nanoscale FDSOI MOSFETs is defined as the voltage at which the sum of the front and the back channel electron densities reaches the doping density of the silicon body. In the case where the front gate oxide is much thinner, the dominance of the front channel is sufficient to explain the experimental results for a wide range of back gate bias. Additionally, the effective conductive path is introduced to derive analytical expression for the threshold voltage. Thus, for thinner front gate oxide, the threshold voltage is defined as the gate voltage at which the electron density at the effective conductive path located at a distance $x = x_c$ from the front interface is equal to the doping density N_A of the silicon body, i.e.:

$$n_i e^{\frac{\varphi_1(x_c,y_m)+\varphi_2(x_c,y_m)V_{tf}}{V_{th}}} = N_A, \quad (1)$$

where $\varphi_1(x_c,y_m)$ and $\varphi_2(x_c,y_m)$ are the channel potential components [9] at the conductive path x_c and the position y_m of the minimum potential, V_{th} is the thermal voltage and n_i is the intrinsic carrier concentration of silicon. Finally, the explicit expression obtained is the following:

$$V_{tf} = V_{fbf} + \frac{V_{th}}{\varphi_2(x_c, y_m)} \ln\left(\frac{N_A}{n_i} e^{-\frac{\varphi_1(x_c, y_m)}{V_{th}}} \right). \quad (2)$$

where $V_{fbf(b)} = \Delta\phi_{f(b)}$ is the flat-band voltage of the front (back) gate. The impact of the back gate bias on the location of the effective conductive path x_c has been modeled with the empirical relations:

$$\frac{x_c}{t_{Si}} = \begin{cases} A_c \exp(V_{gb}/B_c), & V_{gb} \le 0 \\ A_c + 0.04 \cdot V_{gb}, & V_{gb} > 0 \end{cases} \quad (3)$$

which are in qualitative agreement with simulation results of the mean channel position in UTBB FD-SOI MOSFETs [12].

The values of V_{tf} calculated from the model were compared with the experimental values extracted from the transconductance linear extrapolation method [13], validating the model accuracy. The model values of V_{tf} were obtained using $\Delta\phi_f = 0.37$ V for the work function difference for the front gate, including the V_{tf} shift due to quantum confinement [7] and interface traps [9] and $\Delta\phi_b = 0.17$ V for the work function difference for the back gate, $A_c = 0.2$ and $B_c = 3.1$ for the devices of the investigated SOI technology. The parameters $\Delta\phi_f$, $\Delta\phi_b$ A_c and B_c, extracted from the experimental data of V_{tf} versus V_{gb}, are used in the drain current model.

Hereon, the model parameters definitions can be found in Table II. It is common in charge-based models to calculate the drain current based on the linear or exponential dependence of the channel charge density in the strong or in the weak inversion regions of operation, respectively. In order to obtain a single expression for the inversion charge density Q_i, as defined in [14], valid in both regions, we have used an interpolating function of the form:

$$Q_i = \eta_f C_{oxf} V_{th} \ln\left(1 + e^{\frac{V_{gf} - V_{tf} - \eta_f V_y}{\eta_f V_{th}}} \right). \quad (4)$$

Taking into account the entire channel charge distribution instead of the charge sheet approximation, which is not accurate in the moderate inversion region, we can derive the expression for the drain current at any point y in the channel, based on drift-diffusion transport [7]:

$$I_{ds} = W \mu C_{oxf} V_{th} q_i \frac{dV_y}{dy}, \quad (5)$$

Including the carrier saturation velocity and the transversal field effects, the mobility can be approximated as follows [15]:

$$\mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{\upsilon_{sat}} \left| \frac{d\varphi_s}{dy} \right|} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}} \frac{dq_i}{dy}}, \quad (6)$$

Integration from the source to the drain results in the following drain current equation in terms of the normalized charges at the source (q_s) and drain (q_d) electrodes:

$$I_{ds} = \frac{W \mu_{eff} C_{oxf} V_{th}^2 \eta_f}{L + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}} (q_s - q_d)} \left[poly\log\left(2{,}1 - e^{\frac{q_i}{\eta_f}} \right) - \frac{\pi^2}{6} \right]_{q_s}^{q_d}. \quad (7)$$

In order to express the drain current equation explicitly in terms of q_s and q_d, in (7) the dilogarithm function can be replaced by an equivalent 2nd order polynomial expression for compact modeling purpose, obtaining:

$$I_{ds} = \frac{W \mu_{eff} C_{oxf} V_{th}^2}{L_{eff} + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}} (q_s - q_d)} \left[(q_s - q_d) + \frac{1}{2\eta_f} \left(q_s^2 - q_d^2 \right) \right]. \quad (8)$$

which constitutes the basic structure of compact drain current models like BSIM [15], [16]. The μ_{eff} degradation due to the vertical gate field is expressed in terms of q_s as [17]:

$$\mu_{eff} = \frac{\mu_o}{1 + \theta_1 V_{th} q_s + \theta_2 (V_{th} q_s)^2}, \quad (9)$$

where μ_o, θ_1 and θ_2 can be extracted from experimental data at low drain voltage using a modified Y-function method [18]. The parameter θ_2 is correlated to the surface roughness scattering, while θ_1 includes phonon scattering and Coulomb scattering. Taking into account the effect of R_{sd}, θ_1 becomes:

$$\theta_1 = \theta_{1,0} + W \mu_o R_{sd} C_{oxf} / L, \quad (10)$$

In saturation region, based on [19], [20] the channel length shortening ΔL due to the CLM effect can be modelled as:

$$\Delta L = \lambda_f \ln\left(1 + \frac{(V_{ds} - V_{dsat} + 0.05) \tanh(V_{ds}/V_{dsat})^3}{V_E} \right), \quad (11)$$

It should be noted that (8) will lead to an implicit expression for V_{dsat}. Considering that the second charge term in the brackets of (8) is dominant in the above-threshold region, an explicit expression for V_{dsat} can be obtained from the relation $dI_{ds}/dV_{ds} = 0$ yielding:

TABLE II
DRAIN CURRENT MODEL PARAMETERS

Name	Definition	Default value	Units
C_{ox}	oxide capacitance per unit area		F/cm^2
η	interface ideality factor		
V_y	quasi Fermi potential in the channel	0 at source, V_{ds} at drain	V
μ	Electron mobility		cm^2/Vs
μ_o	low-field mobility		cm^2/Vs
μ_{eff}	effective carrier mobility		cm^2/Vs
θ_1 , θ_2	mobility attenuation factors		V^{-1},V^{-2}
$\theta_{1,0}$	linear mobility attenuation coef.		V^{-1}
Q_i	inversion charge density		C/cm^2
q_i	normalized Q_i	$Q_i/C_{oxf}V_{th}$	
L_{eff}	Effective length due to CLM	L - ΔL	cm
φ_s	surface potential		
υ_{sat}	saturation velocity	$\approx 2 \times 10^7$	cm/s
R_{sd}	Series resistance		Ω
λ	natural length		cm
V_E	Fitting parameter		V
V_{dsat}	Saturation drain voltage		V
φ_m	gate metal work function		eV
φ_s	semiconductor work function		eV
λ_w	energy-relaxation length	$2\upsilon_{sat}\tau_w$	cm
τ_w	energy relaxation time constant		s
T	Lattice temperature		K
T_0	Ambient temperature		K
R_{th}	thermal resistance		Ω
K	Thermal conductivity		
r	mobility temperature exponent		

$$V_{dsat}=\sqrt{\left(\frac{\upsilon_{sat}L}{\mu_{eff}}\right)^2+\frac{2q_sV_{th}\upsilon_{sat}L}{\mu_{eff}}}-\frac{\upsilon_{sat}L}{\mu_{eff}}+\frac{q_sV_{th}}{\eta_f}-q_sV_{th}. \quad (12)$$

As V_{tf} is determined at the onset of inversion [9], we found that for a smooth transition from weak to strong inversion, the normalized charge of weak inversion $q_i=Q_i/C_{oxf}V_{th}$ should be obtained with increasing V_{tf} by $2.5\times V_{th}$ and the charge terms of strong inversion with increasing V_{tf} by $5\times V_{th}$.

In order to further improve the accuracy of the model, we include some other important effects, namely the quantum-mechanical (QMEs), VO and the SH effects. As t_{Si} is scaled down below 10 nm, the splitting of the energy bands has to be considered in the model. Due to this splitting, the lowest energy band rises and the carriers need more energy to occupy it, resulting in an increase of the threshold voltage. Thus, the shift in V_{tf} due to quantum confinement is included in the model considering the work function difference as $\Delta\phi=\phi_m-\phi_{snew}$, where ϕ_{snew} the new work function after decreasing ϕ_s by the minimum energy of the lowest conduction sub-band [15]. The shift in V_{tf} due to the quantum confinement according to [7] is $\Delta V_{tf}=0.085+2.178/t_{Si}^2$, where t_{Si} is expressed in nm. Thus, for t_{Si} = 7 nm, the contribution of quantum confinement in $\Delta\phi$ is about 0.129 V.

Positive V_{gb} moves the mean channel position deeper away from the front gate interface into the silicon film [12]. This effect is also taken into account by modifying η_f prior to the drain current calculation. The following back gate bias dependent equivalent thicknesses for the front gate oxide and silicon body are applied to η_f in (8) to refine the drain current calculation [12]:

$$t_{oxf,eq}=t_{oxf}+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}x_c, \quad (13a) \qquad t_{Si,eq}=t_{Si}-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}x_c. \quad (13b)$$

In short-channel transistors, in contrast to the classical drift-diffusion models, υ_{sat} in the saturation region can achieve higher values due to non-stationary effects. This phenomenon is known as velocity overshoot (VO) [21], whose contribution is introduced in a simple way [21]:

$$\upsilon_{sat,vo}=\upsilon_{sat}\left(1+\frac{2\lambda_w}{L}\right), \quad (14)$$

Due to the thin t_{Si}, the SH effect is expected to be significant in short UTBB FD-SOI devices [22]. Experimental evidence for the presence and importance of SH effects in the investigated FD-SOI transistors has been presented in recent works [23]-[24]. Because removal of heat from the channel to the substrate is quick, the temperature rise can be assumed to be uniform throughout the channel given by [22]:

$$T-T_o=R_{th}V_{ds}I_{dso}, \quad (15) \text{ where } \quad R_{th}=\frac{1}{2W}\sqrt{\frac{t_{ox,b}}{K_{ox}K_{Si}t_{Si}}}. \quad (16)$$

Once T is obtained, υ_{sat}, V_{tf} and μ_{eff} have to be recalculated to obtain the drain current at that temperature. For typical temperature rise, the saturation velocity decreases from 1.03×10^7 cm/s at 300 K to 0.96×10^7 cm/s at 380 K, indicating a weak temperature dependence, thus it can be considered constant in our model. Furthermore, it has been demonstrated that in lightly doped UTBB SOI MOSFETs the effect of temperature on the threshold voltage is negligible [25].

In addition to the mobility reduction due to the vertical gate oxide field as described by (9), the carrier mobility decreases with temperature due to increase in phonon scattering. For modeling the SH effect, the effective mobility $\mu_{eff,sh}$ at T is approximated in terms of the effective mobility μ_{eff} at T_o as [26]:

$$\mu_{ef,sh}\approx\frac{\mu_{eff}}{1+\frac{rR_{th}V_dI_{ds}}{T_o}}. \quad (17)$$

In (8), substituting μ_{eff} with $\mu_{eff,sh}$ we get a quadratic expression in terms of I_{ds} the solution of which is given by:

$$I_{ds}=\frac{-A_2+\sqrt{A_2^2+4A_1A_0}}{2A_1}, \quad (18)$$

where $A_0=\frac{W}{L_{eff}}\mu_{eff}C_{oxf}V_{th}^2\left[(q_s-q_d)+\frac{q_s^2-q_d^2}{2\eta_f}\right]$, (19a)

$$A_1=\frac{rR_{th}V_{ds}}{T_o}, \quad (19b) \qquad A_2=1+\frac{V_{th}\mu_{eff}}{\upsilon_{sat,vo}L_{eff}}(q_s-q_d). \quad (19c)$$

IV. Model Validation

The parameters of the device under study, extracted from the transfer characteristics measured at V_{ds} = 30 mV at different back gate voltages using the Y-function method [18], are listed in Table III. The drain current compact model has been verified by comparison with experimental results.

TABLE III
EXTRACTED MOBILITY PARAMETERS FOR L = 30 nm.

V_{gb} (V)	μ_o (cm^2/Vs)	θ_1 (V^{-1})	θ_2 (V^{-2})
-3	93	0.7	0.67
-2	93.5	0.6	0.6
-1	94	0.5	0.6
0	93.5	0.4	0.55
1	95	0.37	0.5
2	93.5	0.4	0.42
3	93	0.4	0.42

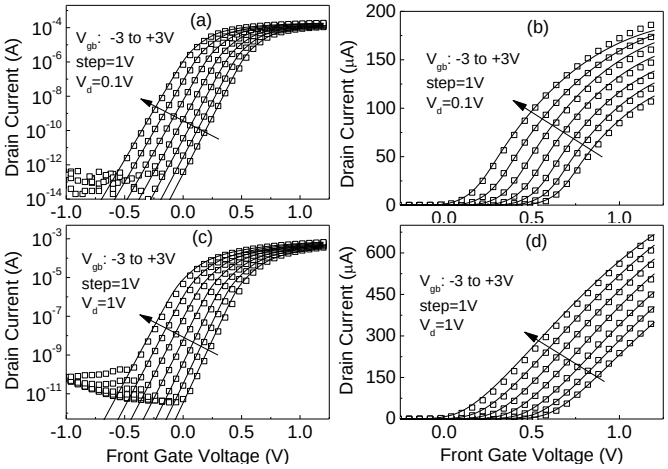

Fig. 1. Experimental (symbols) and modeled (solid lines) transfer characteristics in semi-logarithmic (a, c) and linear (b, d) representation (W = 0.5 μm, L = 30 nm).

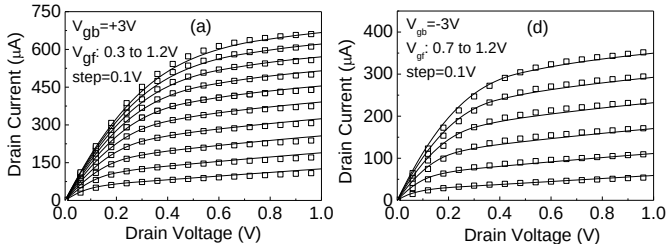

Fig. 2. Experimental (symbols) and modeled (solid lines) output characteristics (W = 0.5 μm, L = 30 nm).

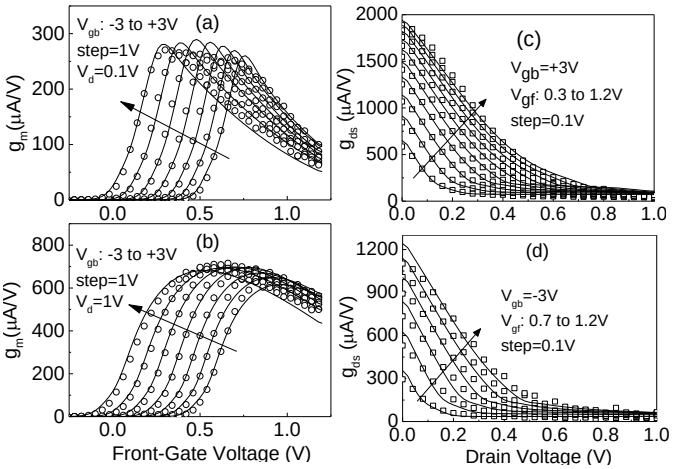

Fig. 3. Experimental (symbols) and modeled (solid lines) transconductance (a, b) and output conductance (c, d) characteristics (W = 0.5 μm, L = 30 nm).

Figs. 1(a)-1(d) present the measured transfer characteristics in semi-logarithmic and linear plots for V_{ds} = 0.1 and 1 V, with back bias voltages V_{gb} varying from -3 to +3 V and Figs. 2(a)-2(b) the output characteristics with parameter the front gate bias V_{gf} and different V_{gb} values. Good agreement between model results and experimental measurements in all operation regimes and for a wide range of back bias is obtained, using fixed values for the parameters: V_E = 0.5 V, λ_w = 100 and 70 nm for $V_{gb} \leq 0$ and $V_{gb} > 0$, respectively and r = 0.5.

In order to further check the accuracy of the model, the small-signal parameters, i.e. the transconductance g_m and the output conductance g_{ds} have been examined. Fig. 3 shows the plots of g_m versus V_{gf} and g_{ds} versus V_{ds}. The agreement between the experimental and modeled results is very good, supporting the accuracy of the compact model. Furthermore, the model has been also validated for a device with larger gate length (L = 240 nm).

V. CONCLUSION

In this paper, we present an analytical compact drain current model for UTBB FD-SOI MOSFETs with back gate control, accounting for saturation velocity, mobility degradation, quantum mechanical, velocity overshoot and self-heating effects. Summarizing, in addition to the mobility parameters (μ_o, θ_1, θ_2) and threshold voltage parameters ($\Delta\phi_f$, A_c, B_c) extracted from experimental data, a limited number of fitting parameters (V_E, λ_w, r) is needed to accurately predict the transfer and output characteristics for a wide range of back gate bias. The good level of accuracy makes the compact model suitable for implementation in circuit simulation tools.

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