A compact delay model for OTFT switches

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***Abstract*—In this paper we present a compact delay model for single switches made using organic transistors. We have started by using a compact model for OTFTs, and we've used the nth-Power law approach to develop our compact model. Simulations results show a mean error below 3%.**

Keywords— delay model, OTFT transistors

I. Introduction

The so-called Flexible, Large Area Organic Electronics (FOLAE) is expected to be one of the next big market hits, and it is, in fact, foreseen (IDTechEx) that will reach around 50 billion € in 2022 [1]. One of the key areas to reach this scenario is that of modelling and characterization of the behaviour of the organic devices.

Some compact models for organic thin film transistors (OTFTs) have already been developed [2-7] and tested, and are already included in some simulation tools [8]. The huge variations which are quite common in FOLAE have also been given some attention in [9].

The above models are all quite precise, but they share a common problem with their counterparts of the classical bulk FET models, namely that they require a lot of computational time that makes them not very suitable for the simulation of large digital circuits. In the classical FET domain, this is solved by developing simple models [10-11] for the power consumption, timing and delay of whole gates, instead of focusing on the devices. In this paper, we have done likewise using a compact OTFT model as the basis, in order to develop a delay model for a switch made using an organic transistor.

The structure of the paper is as follows: in the next Section we present the models of the OTFT and the simplified models we've used. In Section III, we develop and test the delay model and, finally, in Section IV we present some discussion about the results.

II. Model Development

A. OTFT Compact model

Mobility dependence on gate voltage is a critical point in modelling organic TFTs. In the model we have used [3], this dependence is described as:

$$\mu_{FET} = \mu_0 \left(\frac{V_{GS} - V_T}{V_{aa}} \right)^{\gamma_a} = \mu_{FET\,0} (V_{GS} - V_T)^{\gamma_a} \qquad (1)$$

where γ_a and V_{aa} are fitting parameters, V_T is the threshold voltage and μ_0 is the band mobility for the material used in the TFT. Since this last parameter is usually estimated, parameter V_{aa} and μ_0 are compacted into the fitting parameter μ_{FET0}, the low field mobility that has to be adjusted to the experimental value, after γ_a is extracted.

Parameter γ_a is related to the conduction mechanism and is used to describe both an increase and a decrease in mobility due to gate voltage. In the first case we have $\gamma_a > 0$, while in the second case $\gamma_a < 0$. The first behaviour is typical of amorphous and nanocrystalline devices and is related to trap conduction mechanism, while a decrease in mobility is typically related to polycrystalline TFTs when surface roughness scattering starts to be important. In organic TFTs both behaviours have been observed [2]. Thus, extracted fitting parameters can be used to get an insight of the physical mechanisms taking place in the actual devices.

Drain current in the linear and saturation regions in the above threshold regime is modelled [3] as:

$$I_{DS} = \frac{K (V_{GS} - V_T)}{1 + R \cdot K (V_{GS} - V_T)} \cdot \frac{V_{DS} (1 + \lambda V_{DS})}{\left(1 + \left(\frac{V_{DS}}{V_{DSat}} \right)^m \right)^{1/m}} + I_0 \qquad (2)$$

where

$$K = \frac{W}{L} C_{diel}\, \mu_{FET} \qquad (3)$$

In the above equations, W is the channel width, L is its length, C_{diel} is the gate capacitance, R is the source plus drain resistance, m and λ are fitting parameters related to the sharpness of the knee region between linear and saturation and to channel length modulation, respectively.

The saturation voltage is defined using the parameter α_S as:

$$V_{DSat} = \alpha_S (V_{GS} - V_T) \qquad (4)$$

Gate induced leakage current I_0 in equation (2) has been modelled using the same expression than in a classical MOS model, i.e., assuming exponential behaviour of current with respect to gate voltage.

$$I_0 = i_{r0} \cdot e^{-\frac{V_{GS} - V_T - V_{GSX}}{v_{r0}}} \quad (5)$$

where i_{r0} and v_{r0} are fitting parameters.

This model has been implemented in Verilog-AMS inside the Cadence framenwork.

B. nth-Power Law MOSFET Model

The nth-Power law MOSFET Model [10] is a simple empirical model mainly used for analytical analysis at the circuit level. The transistor drain current is given by:

$$I_D = \begin{cases} 0 & V_{GS} \le V_{th} \\ \left(2 - \frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}} I'_{DO} & V_{DS} < V'_{DO} \\ I'_{DO} & V_{DS} \ge V'_{DO} \end{cases} \quad (6)$$

Where I'_{DO} is the drain saturation current:

$$I'_{DO} = I_{DO}\left(\frac{V_{GS} - V_{th}}{V_{DD} - V_{th}}\right)^n (1 + \lambda V_{DS}) \quad (7)$$

Where I_{DO} is a drain current reference, parameter n is the empirical velocity saturation index, and λ describes the channel length modulation. The saturation voltage V'_{DO} is expressed as:

$$V'_{DO} = V_{DO}\left(\frac{V_{GS} - V_{th}}{V_{DD} - V_{th}}\right)^m \quad (8)$$

The parameter V_{DO} is the drain saturation voltage at $V_{GS}=V_{DD}$, while m and V_{th} are empirical parameters. Finally, the threshold voltage model presents a linear dependence with the substrate bias:

$$V_{th} = V_{tho} - \gamma V_{BS} \quad (9)$$

In this model the mobility is considered constant and the velocity saturation effects due to the vertical and horizontal electric fields are modeled through the velocity saturation index n. The main advantages of this model are fast evaluation, simple parameter extraction and simplicity.

C. Characterization of OTFT transistors

In this work we have used a compact model of an OTFT transistor, as described above. Noticing that Eqs 1-3 imply that the current is proportional to $(V_{GS}-V_{th})^n$, we consider a simplification of the nth-Power law model by neglecting the channel length modulation. This way, we are able to obtain a manageable analytic description of input current characteristics. Therefore, the I_D/V_{GS} current characteristics in the over-threshold region are given by:

$$I'_{DO} = I_{DO}\left(\frac{V_{GS} - V_{th}}{V_{DD} - V_{th}}\right)^n \quad (10)$$

Only parameter I_{DO} needs to be extracted, while the transistor threshold voltage and the value of n are obtained directly from the full compact model in section A. A comparison of the delay model and simulations using the full transistor model is depicted in Fig. 1, showing that the transistor behavior is described with good accuracy. The parameter values are V_{th} = -3V, $I_{D0} = 6.6843 \cdot 10^{-8}$ A and n = 3. Notice that in bulk FET the value of n usually ranges between 2 (long-channel devices) and 1 (short-channel devices)

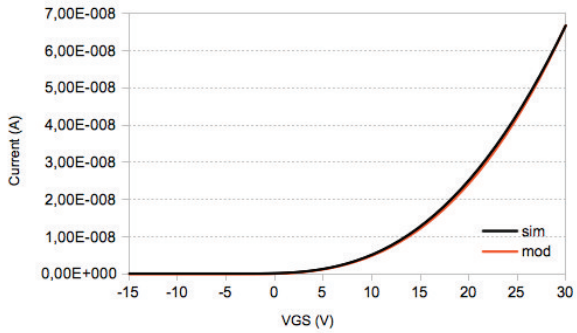

Fig. 1. Comparation betwen the nth-power law model predictions and simulations for a OTFT transistor.

The transistor gate-source voltage response when an input ramp with rise time t_{in} is applied to the device is given by:

$$V_{GS} = V_{in} = \frac{V_{DD}}{t_{in}} t \quad (11)$$

The current expression in the time space takes the form:

$$I_D = I_{DO}\left(\frac{t - t_{on}}{t_{in} - t_{on}}\right)^n \quad (12)$$

where I_{max} and n have the same DC model value and t_{on} is the instant when the transistor starts conducting current, given by:

$$t_{on} = \frac{V_{th}}{V_{DD}} t_{in} \quad (13)$$

Eq. 12 provides a monotonic relationship between current and time, and must be corrected to get current saturation as:

$$I_D = min\left\{I_{DO}\left(\frac{t - t_{on}}{t_{in} - t_{on}}\right)^n, I_{DO}\right\} \quad (14)$$

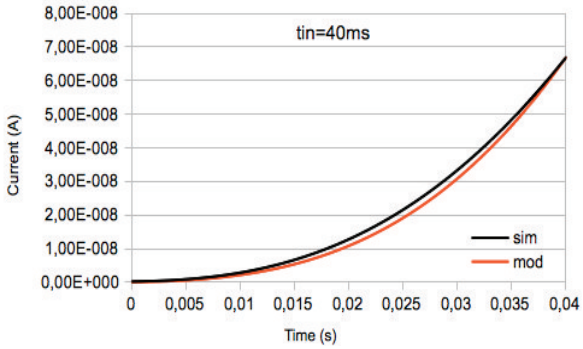

Fig. 2. Comparation betwen the model predictions and simulations of a OTFT transistor for the fastest input rise time t_{in}.

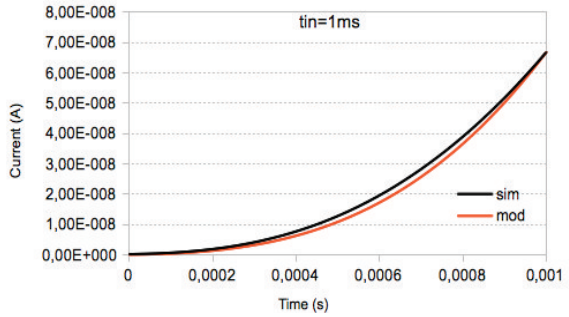

Fig. 3. Comparation betwen the model predictions and simulations of a OTFT transistor for the slowest input rise time t_{in}.

The comparison between the model and simulation results provide a satisfactory description for different input rise time as shown in Figures 2 and 3 where we compare the current behavior for the simulated fastest and the slower values of t_{in}.

III. DELAY MODELING

We obtain the delay model for a simple switch as shown in the circuit in Fig. 4.

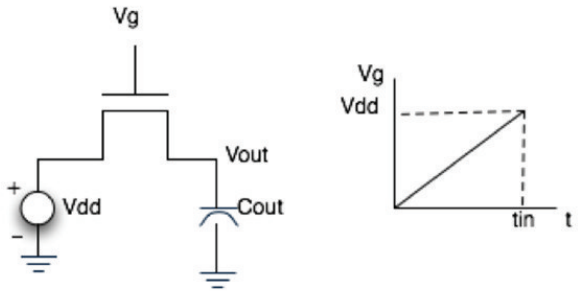

Fig. 4. Circuit under delay analysis. Initially, Vout=0.

The relation between the current of transistor and V_{out} is shown in the Eq (15):

$$\frac{dV_{out}}{dt} = \frac{1}{C_L} I_D \tag{15}$$

where C_L is the overall gate output capacitance having various contributions as C_{out} (the capacitor due to the gates connected to the output node), and the parasitic capacitor of the transistor. Including the drain current expression in Eq. (15) leads to:

$$\int_0^{V_{out}} dV_{out} = \frac{1}{C_L} \int_0^t I_{DO} \left(\frac{t - t_{on}}{t_{in} - t_{on}} \right)^n dt \tag{16}$$

$$V_{out} = \frac{I_{DO}}{C_L} \left(\frac{t - t_{on}}{t_{in} - t_{on}} \right)^{n+1} \frac{(t_{in} - t_{on})}{n+1} \tag{17}$$

In the case of OTFTs, the threshold voltage of transistor can take a negative value and the current is not zero at t=0, but we consider that this current is negligible and we assume that I_D=0 for t=0 to integrate Eq (16).

The gate delay is computed as the t value at which $V_{out}=(V_{DD}/2 - t_{in}/2)$. Defining V_f as the value of Eq. (17) at time $t = t_{in}$, two cases are defined. This is, the current of transistor is defined in two parts, the value between 0 and t_{in}, and the value after t_{in} where the current is constant. Notice that Eq (16) and (17) are only valid for $t<t_{in}$. If this is not the case, then it will be necessary to integrate Eq (16) in two parts, as will be developed below. Taking these considerations into account, we can write the delay expressions as:

A. *Case 1. $V_f > V_{DD}/2$*

In this case, we only have to integrate the first part of the OTFT current because the output voltage reaches $V_{DD}/2$ before $t=t_{in}$. Thus, the delay expression is:

$$t_{d1} = t_{on} + \left[\frac{C_L (V_{DD}/2)(n+1)}{I_{DO}} \right]^{1/(1+n)} (t_{in} - t_{on})^{n/(n+1)} - \frac{t_{in}}{2} \tag{18}$$

B. *Case 2. $V_f < V_{DD}/2$*

Integrating the current in Eq. (16) in two parts, defined by Eq. (14), the delay expression is:

$$t_{d2} = \frac{(V_{DD}/2 - V_f) C_L}{I_{DO}} + \frac{t_{in}}{2} \tag{19}$$

Next the value of C_L is computed. It is worth noticing that the OTFTs have a quite complex behavior with frequency [12], that we have modeled using Eq. (20).

$$C_L = a(t_{in})^b \tag{20}$$

where a and b are constants depending on the technology and the transistor dimensions. Taking into account the variation of C_L with the rise time of the input signal and considering Eq (20) for this dependence, we have computed the delay times for several input rise times. Figure 5 shows the comparison between the simulated and modeled values of delay. For the worst case the relative error is 5.6% and for the best case is 0.3%, with a mean error of 2.7%.

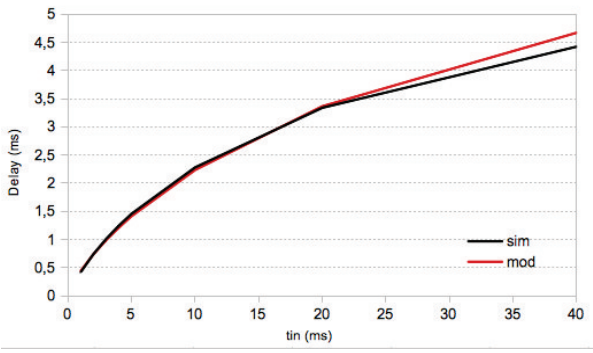

Fig. 5. Comparison between simulated (black) and modelled (red) delay times for a 1pF load.

IV. Conclusion

In this paper we have developed a very simple model for the delay time of a single transistor switch using an organic device. This model provides a very simple analytical expression, which can be seen in Eqs. (18) and (19). This model also takes into account the variation of the capacitance with the frequency, and shows a mean error below 3%.

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References

[1] R Das and P Harrop, "Organic & printed electronics--forecasts, players & opportunities 2012-2022," techreport 2012

[2] M. Estrada, et. al., “Mobility model for compact device modelling of OTFTs made with different materials”, Solid-State Electronics, vol 52, no 5, pp 787-794, 2008

[3] M. Estrada, et. al., “Modeling the behavior of charge carrier mobility with temperature in thin-film polymeric transistors”, Microelectronic Engineering, vol 87, no 12, pp 2565-2570, 2010

[4] B Iñiguez, et al., "Compact modeling of organic thin-film transistors," , 2010, pp. 1268-1271

[5] M Fadlallah, et al., "Modeling and characterization of organic thin film transistors for circuit design," Journal of Applied Physics, vol. 99, p. 104504, 2006

[6] L Fortuna et al., "On the way to plastic computation," Circuits and Systems Magazine, IEEE, vol. 8, pp. 6-18, 2008

[7] Marinov, et al., "Organic thin-film transistors: Part I: Compact DC modeling," Electron Devices, IEEE Transactions on, vol. 56, pp. 2952-2961, 2009

[8] S Mijalkovic et al., "Modelling of organic field-effect transistors for technology and circuit design," , 2008, pp. 469-476

[9] R. Picos et al. “Effect of process variations on an OTFT compact model parameters”, International Journal of High Speed Electronics, vol 20, no 40, pp 815-828

[10] Takayasu Sakurai and Richard Newton, “ A Simple MOSFET Model for Circuit Análisis”. IEEE Transactions on Electronic Devices, vol. 38, pp 887-894, Apr 1991

[11] J.L. Rosselló, C. de Benito, J. Segura, ”A Compact Gate-Level Energy and Delay Model of Dynamic CMOS Gates”, IEEE Transactions on Circuit and Systems, vol.52, pp.685-689, 2005

[12] Castro-Carranza, A.; Estrada, M.; Nolasco, J.C.; Cerdeira, A.; Marsal, L.F.; Iñíguez, B.; Pallarès, J., "Organic thin-film transistor bias-dependent capacitance compact model in accumulation regime," Circuits, Devices & Systems, IET , vol.6, no.2, pp.130-135, March 2012