

14nm Fully Depleted SOI: Technology, Devices and Scalability

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Abstract— High-speed circuits, as well as highly-efficient power management and process compensation techniques were already demonstrated on planar FDSOI [1-3]. This is enabled by CMOS devices of high-performance, low-variability, high body-factor, as evidenced at the 28nm and 14nm nodes [4-5]. In this abstract, we will start describing the 14nm FDSOI technology and devices we have developed, and then focus on some technology knobs that could be useful in the future in order to scale this architecture down to the 10nm node, namely the body and buried oxide scaling, the strain-SOI substrates (sSOI) and the gate last introduction.

I. INTRODUCTION

The 28 nm FDSOI technology started production in 2013 [4]. The early target of 30% boost in performance, compared to the 28nm bulk technology has been demonstrated on processed products. This technology can address both high performance and low power / low voltage applications. Indeed, a 28 nm FDSOI Processor (CPU) has been demonstrated to run at 3 GHz for a 1.3 V supply voltage (V_{dd}), 1 GHz for 0.6 V, still 300 MHz at 0.5 V [1]. This evidences the high potential for this FDSOI process for one of the key application fields for the next market challenges: Low Voltage applications for the handheld, the mobile or the Internet-Of-Things business. The 14nm FDSOI technology extends this offer to even more performance, with a 100mV supply voltage reduction [5]. In this abstract, we will start describing this 14nm FDSOI technology and devices we have developed, and then focus on some technology knobs that could be useful in the future in order to scale this architecture down to the 10nm node, namely the body and buried oxide scaling, the strain-SOI substrates (sSOI) and the gate last introduction.

II. 14NM FDSOI TECHNOLOGY AND DEVICES

The 14nm FDSOI technology we have developed, features a 90nm minimal contacted poly pitch and 64nm Metal1 pitch, two V_T flavors (LVT and SLVT), a minimum gate length of 20nm, a 6nm channel and 20nm buried oxide (BOX) thicknesses, a dual Si/SiGe channel (directly on insulator) and dual SiCP/SiGeB sources/drains. The strained-SiGe channel of the pMOSFETs (cSiGe) is realized by Ge-enrichment process before the Shallow Trench Isolation patterning in order to get uniform channel. A 1% compressive strain has been experimentally measured in the 6nm thin cSiGe channel (25%

Ge amount). This SiGe channel and SiGeB source/drain combination is one of the main sources of performance improvement w.r.t. 28nm, together with the gate stack optimization and Equivalent Oxide Thickness scaling. This leads to an effective current of $I_{eff}=330\mu A/\mu m$ and $405\mu A/\mu m$ at a V_{dd} of 0.8V and an OFF-state current $I_{off}=20nA/\mu m$ are demonstrated for both the pMOS and nMOS transistors in a ring oscillator (RO) environment (Fig.1). In addition, the poly-bias capability (resulting in up to 34nm gate length in a 90nm gate pitch) results in a more than 3 decades reduction of leakage. As a result, 14FDSOI technology demonstrates a -20% delay gain on a Fan-Out 3 (FO3) inverter Ring Oscillator at the same static leakage and a 100mV V_{dd} reduction (0.8V vs 0.9V) over the 28nm FDSOI technology (Fig.2).

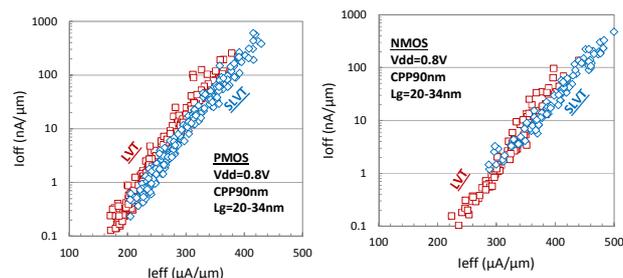


Fig. 1. I_{eff} vs. I_{off} at $V_{dd}=0.8V$ for p & nMOSFETs at $W=0.17\mu m$.

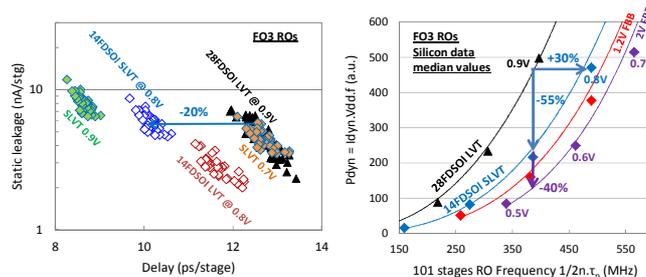


Fig. 2. FO3 RO delay vs I_{stat} for 28FD and 14FD at different V_{dd} (left); frequency vs P_{dyn} for various V_{dd} and various FBB (right).

The specificity of planar FDSOI, compared to FinFETs is its marvelous capability to bias the wells with high efficiency on the front-gate threshold voltage and, in turn, the transistor / circuit gate performance. To enable this option, a process module was developed in 28nm and optimized for 14nm, creating bulk areas, before the Shallow Trench Isolation (STI) module. These bulk regions provide a space for well taps,

passive devices and ESD FETs. Fig.2 illustrates the dramatic frequency boost using Forward Body Bias (FBB). The devices running at $V_{dd}=0.6V$ with a 2V FBB are as fast as devices running at $V_{dd}=0.8V$ with no back bias. Doing this, you can reach your timing target while reducing the supply voltage of your block / circuit and thus the dynamic power defined by $P_{dyn}=I_{dyn}\times V_{dd}\times f=C_{eff}\times V_{dd}^2\times f$ with I_{dyn} the dynamic leakage, f the frequency of the circuit, C_{eff} the effective capacitance. In the previous example relative to Fig.2, using 2V FBB enables reducing the dynamic power by 45% at a given speed.

III. HOW TO SCALE FDSOI BELOW 14NM?

The technological knobs to scale the FDSOI technology below 14nm are relative to both the electrostatics and the carrier mobility. As far as the electrostatics is concerned, the Equivalent Oxide Thickness (EOT) has to be reduced, while ensuring a good reliability. For pMOSFETs, the increase of the Ge content of the cSiGe channel helps optimizing this EOT/reliability tradeoff [6]. On planar FDSOI, the other electrostatic ingredient is the channel thickness (T_c), which should more or less follow the rule of thumb of $T_c=L_{gmin}/4$ with L_{gmin} the minimum gate length of the technology. The BOX thickness (T_{BOX}) down-scaling is useful but of the second order to improve the electrostatics, while it is the key factor to adjust the body bias efficiency in planar FDSOI technology. The scaling of both T_c and T_{BOX} will be mandatory if the minimum gate length is itself down-scaled.

Now, dimension scaling is no longer sufficient to guaranty a boost of performance superior to 20% from a node to the next one. Carrier mobility boosters are required. For pMOSFETs, one can think about changing the crystalline orientation of the SOI. In this case, (110) planes are of interest, at least for long channel devices (Fig.3). Alternatively, changing the channel orientation (with a 45° in plane SOI rotation) could also boost the long channel hole mobility (Fig.3). However, in terms of strain management, the long channel mobility is not the relevant electrical parameter. One should pay a great attention to the local layout effect and specially, the evolution of the apparent mobility with the gate length and width (Fig.3), as well as its variation with the extension length (i.e. the distance between the gate and the STI in the source/drain direction). Taking the layout effects into account, for pMOSFETs, SiGe channel, SiGeB source/drain and compressive contact etch stop layers in the (110) <110> direction are the best combination. For nMOSFETs, different technological solutions have been assessed, especially based on strain memorization techniques [7]. None has experimentally demonstrated a clear advantage yet, except strain-SOI substrates (sSOI). This substrate itself brings enough performance boost to ensure a one-node scaling (+20-30% performance increase for nMOSFETs due to tensile strain) [8]. Moreover, like cSiGe channel, its benefit is even higher, narrower the transistors (Fig.3). Challenges related to sSOI integration may be i) the compatibility with the aforementioned preferred boosters of hole mobility and ii) the substrate readiness/quality. The gate last integration on planar FDSOI could be another strain booster because it leverages not only a low thermal budget for EOT and threshold voltages optimization, but also a strain increase during the final gate formation (Fig.4) [9]. Anyway, the best solution to induce a

strain in the transistors will be obtained by smart design layouts and process integration in order to match the best strain configuration: uniaxial longitudinal strain for both n&pMOSFETs (Fig.5).

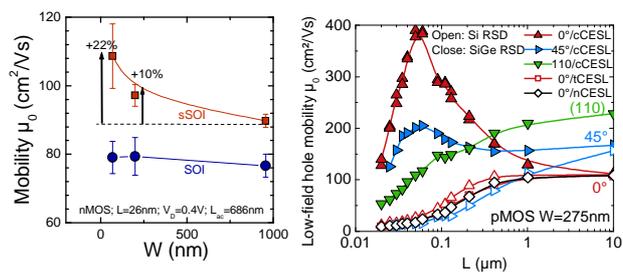


Fig. 3. Low field mobility vs. transistor width (W) for SOI and sSOI nMOSFETs (left) and vs. gate length for pMOSFETs with different surface/orientation and source/drain configurations (right).

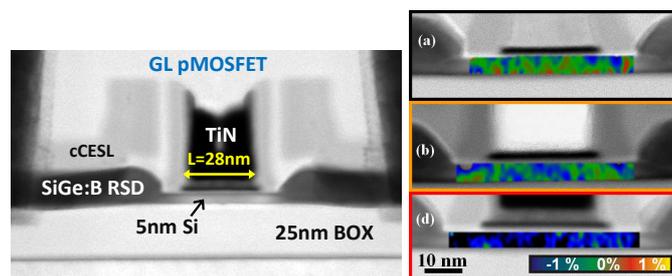


Fig. 4. TEM picture of a gate last pMOSFET with *in-situ* boron doped SiGe raised source/drain and compressive Contact Etch Stop Layer (cCESL) (left) and 2D in-plane longitudinal strain mapping after CMP (a), PolySi removal (b) and back-end processes (d) (right).

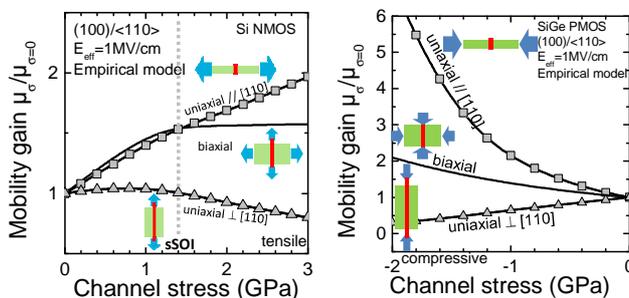


Fig. 5. Model of electron mobility variation in Si (left) and hole mobility variation in SiGe (right) vs. stress based on exp. piezoresistance coefficients [8 and reference therein].

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