Static Power Estimation of Digital Circuits by means of Power Contributors.

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***Abstract* - This paper examines the efficiency of the power contributor approach in modeling the leakage currents and static power consumption of CMOS cells. Different CMOS cells included in the NaNGate library are decomposed into power contributors and all the leakage currents running through their terminals are modeled. The results reveal the overall efficiency of the method.**

Keywords - CMOS static power, modeling, power contributors.

I. INTRODUCTION

The modern trends in digital circuit design require a fast and reliable estimation of the static power consumption and the leakage currents running through the cells. These phenomena are comparable with their dynamic counterparts, making them significant design parameters, in low power and/or high density implementations.

A complete characterization of a design library in terms of the above phenomena requires hours of simulations and enough modeling effort. For a given cell, all input and power supply leakage currents must be simulated and modeled for different design corners. The same holds for static power consumption. Also, because of the state dependent nature of these quantities, the above procedure must be repeated for all possible input combinations. Therefore, it is preferred to seek a method that can facilitate the above process, and can be easily applicable to different fabrication processes.

The Power Contributor approach was presented by Dhanwada et al [1] and came to speed up this procedure in a systematic way. Any cell, for a given state, can be decomposed into smaller and easier to handle circuits, called Power Contributors (from now on PCs). Moreover, these elementary circuits can be used again and again as they correspond to multiple cells, thus reducing significantly the characterization effort.

This paper studies the efficiency of the PC approach by application on different cells of the NaNGate library [2] and expands the existing work done so far by the authors. The transistor model used in this library is the PTM CMOS model at 45nm from Arizona State University [3]. All the data needed for model generation and testing, came from simulations conducted by the HSPICE I-2013.12-1 simulator.

I. THE POWER CONTRIBUTORS APPROACH

In order to illustrate the method, two cells from NaNGate library where picked: the NAND2_X1 at state "11" and the AOI21_X1 gate at state "001" (Fig.1).

The first stage of the approach is to identify all the well-defined voltage levels, at the circuit's nodes. These levels are denoted with "0" or "1" and they correspond to GND or VDD potential. Then each subcircuit laying between these levels (denoted with a red frame in Fig.2) is connected to a separate supply terminal, making the above cells to collapse into smaller ones, as shown in Fig.3. These subcircuits are the PCs of the NAND2_X1 and AOI21_X1 cells for their given state.

The naming of these PCs comes as is, from Ref. [1]. A "C" prefix stands for channel leakage – i.e. the PC has a subthreshold current running through the channel and also a gate leakage running through the gate. A "G" prefix stands for gate leakage – i.e. the corresponding PC has only a gate current leakage running through the gate. Finally, the "P" and "N" suffixes stand for PMOS and NMOS respectively.

The next stage of the method is to create a suitable model for every current that runs through the PCs. For the PCs in figure 3, the corresponding macromodels are derived by nonlinear regression:

$$I_{GP} = 2.59593\times10^{-19} e^{-4.68241/V} + 9.55531V \\ (T+2745.43)(W-6.66667)V^{-9.5} \quad (1)$$

$$I_{GN}=9.9568310^{-16} e^{2.33018V}(T+113.68)(W-9.99702)V^{3.62} \quad (2)$$

$$I_{CP}^{GATE} = 3.7548\cdot10^{-15} e^{-0.968237/V} + 3.59696V\,(W-6.68094) \quad (3)$$

$$I_{CP}^{CHANNEL} = 2.58757\cdot10^{-11} e^{-2456.25+(788.781+1.74201T)V/T}(W-6.6929)/V \quad (4)$$

$$I_{CN}^{GATE} = 9.56293\cdot10^{-14} e^{3.63763V} V^2 (W-10.0001) \quad (5)$$

$$I_{CN}^{CHANNEL} = 1.42922\cdot10^{-11} e^{-2274.29+(619.481+0.46047(T-1))V/T-1} \\ (T-121.924)(W-10.0105) \quad (6)$$

Units: T[K], W[nm] (NMOS), V[V] (V_{DD}).

The final step is the combination of all the above macromodels, into suitable expressions describing every static current that runs through the cell's terminals. For instance, the gate leakage in A2 terminal for the NAND2_X1:

$$I_{A2} = I_{CP}^{GATE} + I_{GN} \quad (7)$$

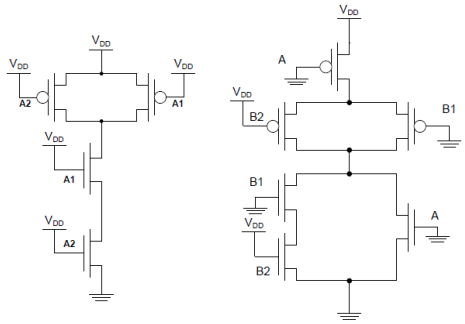


Fig. 1. The NAND2_X1 and AOI21_X1 cells.

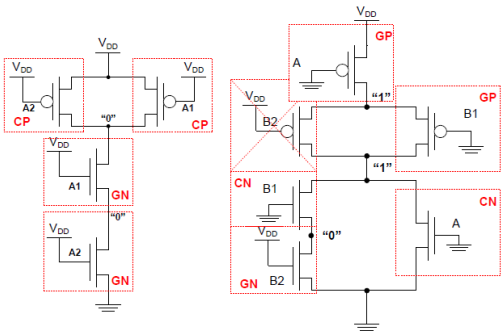


Fig. 2. PCs from NAND2_X1 and AOI21_X1 cells. Each red frame denotes the name and the connectivity of each PC. The double strikethrough line means that the corresponding MOS does not does not taken into account.

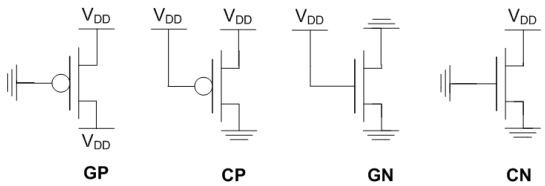


Fig. 3. PC embodied in multiple cells such as the INV_X1, NAND2_X1, NOR2_X1, AOI21_X1.

and for V_{DD} terminal:

$$I_{VDD} = 2I_{CP}^{CHANNEL} \tag{8}$$

whereas the gate leakage in A terminal for AOI21_X1 cell:

$$I_A = I_{GP} + I_{GN} \tag{9}$$

and for V_{DD} terminal:

$$I_{VDD} = 2\left(I_{GP} + I_{CN}^{CHANNEL} + I_{CN}^{GATE}\right) \tag{10}$$

All the above equations produce a mean relative error less than 2%, compared to the corresponding values from simulation. The maximum relative error seldom exceeds 2%. Similar expressions hold for every other quantity in the circuits.

Finally, the PCs method was used to calculate the static power consumption of INV_X1, NAND2_X1, NOR2_X1 cells for the nominal case of W_{NMOS}=100nm, V_{DD}=1V and T=25^{O}C [4]. For every combination of input states and for every cell, the relative error between the actual power leakage and the total power leakage obtained by the PC models is less than 0.02%. This fact reveals the outstanding performance of this method.

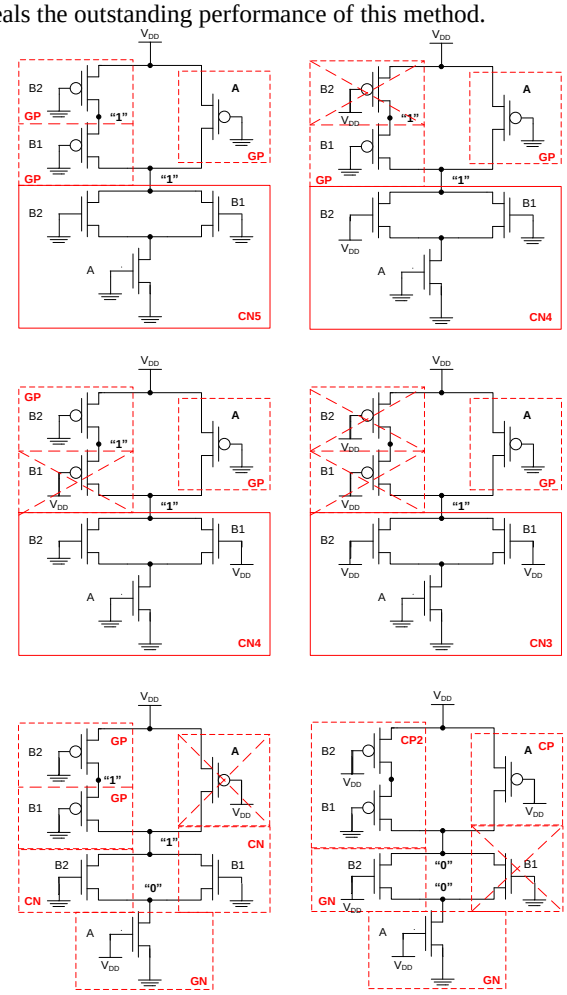
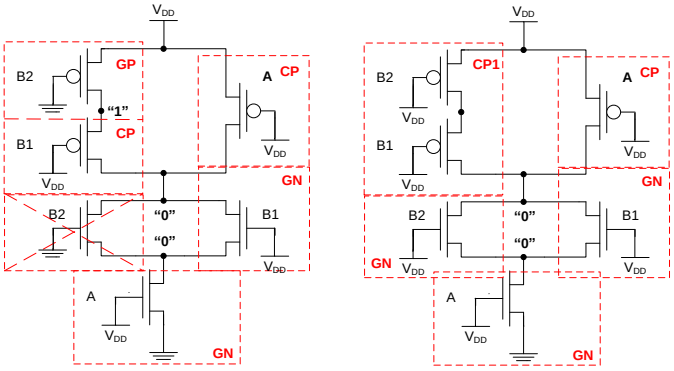


Fig. 4. The OAI21_X1 cell, along with the corresponding PCs, at states "000", "010","011","100","101".

Fig. 5. The OAI21_X1 cell, along with the corresponding PCs, at states "110", "111".

II. Application of PCs into different cells

Until now, the PC approach was applied into INV_X1, NAND2_X1, NOR2_X1, AOI21_X1, OAI21_X1, NAND3_X1 and NOR3_X1 elementary cells. The decomposition of the first three was presented into [4]. The decomposition of the OAI21_X1 cell is shown in figures below:



The macromodels used to describe all the currents in the PCs, CN3,CN4 and CN5, have the functional form:

$$I^{GATE} = A_0(W - w_1)e^{a_1/V + a_2 \cdot V} V^{b_0} T^{b_1} \quad (11)$$

$$I^{CHANNEL} = A_0(W - w_1)e^{\frac{a_1 + (a_2 + a_3 T)V}{T}} V^{b_0} T^{b_1} \quad (12)$$

Depending on the case, these equations can change slightly, by replacing the power dependencies with linear or sigmoidal functions.

Finally, it is worthy to note that the above expressions, in their final form slightly exceed a maximum relative error of 2%. The same holds for every final expression that describes the leakage currents running through the modelled cells.

I. Final Conclusions

As demonstrated, the PC approach is a systematic and very accurate method to "synthesize" expressions that can characterize a cell library. A standard modeling approach of the INV_X1, NAND2_X1, NOR2_X1, AOI21_X1, OAI21_X1, NAND3_X1 and NOR3_X1 cells for every state requires 232 different equations. The PC approach in turn, requires only 76 different equations, for a full characterization.

This in fact means that the PC approach has reduced the modeling effort by roughly 67%. To conclude, the power contributor approach has proven to be an extremely efficient method for static power modeling compared to other methods such as the cascade analysis.

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